Code No: R5210505 R5

II B.Tech I Semester(R05) Supplementary Examinations, December 2009
COMPUTER ORGANIZATION
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) What are the functional units?. Are they always processors? [6]
   (b) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous. [10]

2. Design register selection circuit to select one of the four 4-bit registers content on to bus. Give fuller explanation. [16]

3. (a) Why do we need subroutine register in a control unit?. Explain. [8]
   (b) Support or oppose the statement ? the control unit is a firmware?. [8]

4. Draw a owchart to explain how two IEEE 754 oating point numbers can be added, subtracted and multiplied. Assume single precision numbers. Give example for each [16]

5. (a) What is Locality of Reference? Explain [6]
   (b) What is the need of Replacement Algorithms for a Cache Memory? Explain any two Cache Replacement Strategies. [10]

6. (a) What is daisy chaining? Explain with neat sketch.
   (b) What is parallel priority interrupt method? Explain with neat sketch. [8+8]

7. Explain the following with related to the Instruction Pipeline
   (a) Pipeline con icts
   (b) Data dependency
   (c) Hardware interlocks
   (d) Operand forwarding
   (e) Delayed load
   (f) Pre-fetch target instruction
   (g) Branch target bu er
   (h) Delayed branch [8×2=16]

8. (a) Explain the working of 8 x 8 Omega Switching network.
   (b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch [8+8]