Code No: R5310201 R5

III B.Tech I Semester(R05) Supplimentary Examinations, December 2009

COMPUTER ORGANIZATION

(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Control Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions

All Questions carry equal marks

1. (a) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous.

   (b) Explain about daisy chain based bus arbitration. [16]

2. (a) What is meant by instruction set architecture?. Explain in detail [10]

   (b) Which factors decides instruction format (size). Explain in details. [6]

3. (a) Explain the variety of techniques available for sequencing of microinstructions based on the format of the address information in the microinstruction. [8]

   (b) Hardwired control unit is faster than microprogammed control unit. Justify this statement. [8]

4. (a) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit multiplications. [8]

   (b) Explain single precision and double precision calculations. In general how many bytes are used for both and what is the precision we get. Give some examples where double precision calculations are needed. [8]

5. Explain the following:

   (a) Magnetic Tape Systems

   (b) Optical Disc

   (c) DVD Technology. [5+5+6]

6. (a) Explain bit oriented and character oriented protocols in serial communication.

   (b) What are the di erent issues behind serial communication? Explain. [8+8]

7. What is pipelining? Explain pipeline processing with an example. [16]

8. (a) Explain the working of 8 x 8 Omega Switching network.

   (b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch. [8+8]