

IV B.Tech I Semester(R05) Regular & Supplementary Examinations, December 2009
EMBEDDED SYSTEMS
(Common to Computer Science & Engineering, Information Technology, Electronics &
Control Engineering and Computer Science & System Engineering)
Time: 3 hours Max Marks: 80
Answer any FIVE Questions
All Questions carry equal marks

KOTTAM
INSTITUTIONS

1. (a) What is an embedded system? Why is it so hard to define?
(b) List the applications of embedded systems. [8+8]
2. Design a 3-bit counter that counts the following sequence: 1,2,4,5,7,1,2,... start from a state diagram, draw the state table, minimize the logic, and draw the final circuit.[16]
3. (a) Explain the stages of Instruction Execution?
(b) What is meant by superscalar and VLIW architectures. [8+8]
4. State the need for more functional units in digital signal processor. [16]
5. Briefly discuss three computation models commonly used to describe embedded systems and their peripherals.[16]
6. (a) Explain rate monotonic priority scheduling algorithm with an example.
(b) Explain deadline monotonic priority assignment scheduling algorithm with an example. [8+8]
7. List and describe three general approaches to improving designer productivity. [16]
8. Explain in detail about intellectual property cores. [16]

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1. (a) What is an embedded system? Why is it so hard to define?
(b) List the applications of embedded systems. [8+8]
2. (a) What is a combinational circuit? Explain the procedure of combinational logic design?
(b) Take any logic expression and explain the combinational logic design. [8+8]
3. Describe why a general-purpose processor would cost less than a single-purpose processor you design yourself.[16]
4. Draw and explain architectural features of TMS 320C25. [16]
5. Explain how to compute state machines in sequential programming language. [16]
6. Explain in detail about data flow model with an example. [16]
7. Describe each tool that has enabled the elevation of software design and hardware design to higher abstraction levels.[16]
8. (a) What is hardware/software co-simulation?
(b) What is a key method for speeding up such simulation? [8+8]

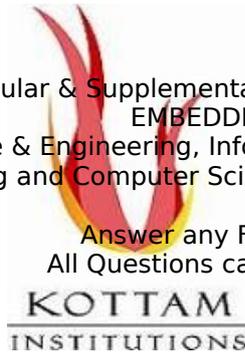
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1. (a) What is a trade-off? Explain in detail.
(b) Explain about design productions gap. [8+8]
2. (a) Explain why NAND and NOR gates are more common than AND and OR gates.
(b) Realize all the gates using NAND and NOR gates. [8+8]
3. Explain the following three application specific instruction set processors.
(a) Microcontroller
(b) Digital signal processor
(c) Less -general ASIP environment. [6+5+5]
4. State the need for more functional units in digital signal processor. [16]
5. (a) What are the models commonly used for describing embedded systems?
(b) State differences between a computation model and a language, and also between a textual language and a graphical language.[8+8]
6. (a) Explain rate monotonic priority scheduling algorithm with an example.
(b) Explain deadline monotonic priority assignment scheduling algorithm with an example. [8+8]
7. List and describe three general approaches to improving designer productivity. [16]
8. Explain in detail about intellectual property cores. [16]

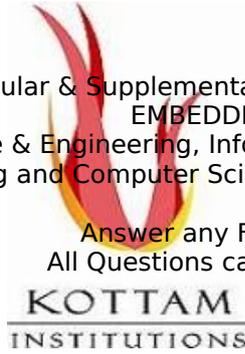
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1. (a) Define a system? Define an embedded system Differentiate this with desktop system.
(b) Classify the embedded systems and Mention few applications on each. [8+8]
2. (a) What is a combinational circuit? Explain the procedure of combinational logic design?
(b) Take any logic expression and explain the combinational logic design. [8+8]
3. Describe why a general-purpose processor would cost less than a single-purpose processor you design yourself.[16]
4. (a) Give the bus structure for digital signal processor.
(b) Explain the need for more buses in DSP architecture. [8+8]
5. (a) Using sequential control model explain an elevator controller system.
(b) Define the following terms:
Finite state machines, concurrent processes, real-time systems, and real-time operating systems.
[8+8]
6. Explain different states and operations in concurrent processes model. [16]
7. Design a circuit for the expression $F=abc'd'+a'cd+ab'cd$ with minimum gates using two level logic minimization.[16]
8. (a) What is hardware /software co-design?
(b) Explain temporal and spatial thinking in hardware/software co-design? [8+8]