Code No: R5320404 **R5**

**III B.Tech II Semester(R05) Supplementary Examinations, May 2010**
**VLSI DESIGN**
**(Common to Electronics & Communication Engineering and Bio-Medical Engineering)**
**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. With neat sketches explain the Ion -lithography process. [16]
2. (a) Derive the relationship between drain to source current $I_{ds}$ and drain to source voltage $V_{ds}$ in non saturation and saturation region
   (b) Sketch the $I_{ds}$ versus $V_{ds}$ graph for enhancement mode device. [10+6]
3. (a) what is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
   (b) What are the effects of scaling on $V_t$?
   (c) What are design rules? Why is metal- metal spacing larger than poly -poly spacing. [8+4+4]
4. (a) what are the advantages of transmission gates over pass transistors?
   (b) Implement the following using transmission gates
      i. 2 to 1 multiplexer.
      ii. OR gate. [5+6+5]
5. Develop a model of word line decoder delay for a RAM with $2^n$ rows and $2^m$ columns. Assume true and complementary inputs are available and that the input capacitance equals the capacitance of one of the columns of H=$2^m$. Use static CMOS gates and express result in terms of n and m. [16]
6. (a) Draw and explain the FPGA chip architecture.
   (b) Draw and explain the AND/NOR representation of PLA. [8+8]
7. (a) Compare the behavioral and structural styles of VHDL with example.
   (b) Explain the method of Binary composition for chip routing with suitable example. [8+8]
8. Explain the following with respect to CMOS testing: [4×4=16]
   (a) ATPG
   (b) Fault simulation
   (c) Statistical Fault Analysis
   (d) Fault Sampling.



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